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Abstract
In this thesis, a DVI (Digital Visual Interface) receiver applicable to the TFT-LCD panels with VGA standard is presented. For Data recovery system is oversampled three times using 30 multiphase clocks .The 30 bits of oversampled data are processed in parallel by the DPLL to extract the phase information from the incoming data patterns. Total of 10 bits of data are recovered in each cycle by selecting the center bits among 30 oversampled bits. For the frame synchronization, out-of-band transition detectors are designed to detect the preamble signals. For the data decoder, an efficient 10-to-8 bits decoder is designed to make the output signals applicable to the source driver. The receiver is implemented by the TSMC 0.35um 1P4M CMOS technology. Experimental results show that the layout area is 0.76 0.75mm2 with the power consumption of
93 mW.
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